REMARKS/ARGUMENTS

The Office Action has been carefully considered. It is respectfully submitted that the issues raised are traversed, being hereinafter addressed with reference to the relevant headings appearing in the Detailed Action section of the Office Action.

Claim Rejections – 35 USC § 103

On page 2 of the Office Action, the Examiner rejects claims 1 to 6 as being unpatentable over Mehrotra et al (US Patent No. 6,145,054). Reconsideration and withdrawal of this rejection is respectfully requested in light of the following comments.

Obviousness can only be established by combining or modifying teachings of the prior art to produce the claimed invention where there is some teaching, suggestion or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art.

In particular, the MPEP states at §2143 "*Basic Requirements of a Prima Facie Case of Obviousness*" that:

> "*... three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations.*
>
> *The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, not in applicant's disclosure. In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).*"

On page 3 of the Office Action, the Examiner states:

> "a processor connected to the cache via a cache bus (Fig 1: #102, processor connecting with the cache #105; column 1 lines 60-68); a memory interface (Fig 4) connected to the cache via a first bus (Fig 1: #107, main memory and #105 cache) and to the processor via a second bus (Fig 1: #102), the first bus being wider than the second bus or the cache bus (Mehrotra's Fig 6B, column 13 lines 62 to column 14

lines 15 describes the cache using the read port 8 bytes wide to supply data back to the processor and using fill port 32 bytes wide for data returning to memory); and memory connected to the memory interface via a memory bus (Fig 4: #107)"

The Examiner considers that the write/fill port 32 byte in length (as shown in Figure 6B) corresponds to a first bus connecting a memory interface to the cache, as recited in claim 1. The Examiner also considers that the read ports 8 bytes in length (as shown in Figure 6B) corresponds to a cache bus connecting the cache to the processor, as recited in claim 1.

However, Mehrotra et al does not disclose or suggest having a second bus connecting the processor to a memory interface, and having a memory bus connecting the memory to a memory interface, as recited in the present claim 1. Furthermore, the disclosure in Mehrotra et al does not provide any motivation or suggestion as to how the system can be modified to include a second bus and a memory bus as recited in claim 1 of the present application.

On page 3 of the Office Action, the Examiner states:

"(c) sending, from the memory interface and via the first bus, the first data and additional data, the additional data being that stored in the memory adjacent the first data (Mehrotra's column 9 lines 1-5, cache fill operation)"

The description at column 9 lines 11 to 23 clarifies the cache fill operation described at column 9 lines 1 to 5. When the processor attempts to read data from memory, it first checks if a valid cache line for that memory location exists in the cache, such as by checking a status bit associated with each cache line. In the event of a cache miss, a cache line is allocated, and data for the requested memory location is returned from higher cache levels or main memory and is stored in the allocated cache line. Mehrotra et al does not disclose or suggest sending first data and additional data as recited in the present claim 1. Furthermore, the disclosure in Mehrotra et al does not provide any motivation or suggestion as to how the system can be modified to include sending first data and additional data as recited in claim 1 of the present application.

Present claims 2 to 6 depend, at least in part, on claim 1. Accordingly, the above remarks also apply to present claims 2 to 6.

Accordingly, the Applicant respectfully submits that the first basic requirement of a prima facie case of obviousness has not been met to reject the claims as unpatentable, as per MPEP §2143.

Very respectfully,

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